Amendments to the Drawings:

The attached replacement sheets of drawings include changes to Figs. 4 & 5 and replace the original sheets including Figs. 4 & 5.

In Figure 4, a separate reference numeral "54" has been included for each arrow, and the arrows corresponding to number 54 are now more neatly illustrated.

In Figure 5, a reference numeral "64" has been added to each AVAILABLE line.

Attachments following last page of this Amendment:

Replacement Sheet (5 pages)

REMARKS

Claims 1-46 are pending, with claims 1, 15, 23, 32 and 39 being independent. Claims 1, 10, 11, 13, 15-17, 23, 32 and 39 have been amended. No new matter has been added. Reconsideration and allowance of the above-referenced application are respectfully requested.

Specification:

The title ("SELECT-FREE DYNAMIC INSTRUCTION SCHEDULING") stands objected to as allegedly being not descriptive of the invention. However, the title is generally descriptive of the invention. As described in the specification: "With select-free scheduling logic, an instruction speculates that it will be selected for execution. The instruction asserts the AVAILABLE lines for its wakeup array entries before selection of the instruction is confirmed." (See the present specification at page 11, lines 5-9.) Thus, the instruction scheduling is select-free. In view of the remarks and amendments made, withdrawal of the objection to the title is respectfully requested.

The abstract stand objected to for various informalities. The abstract has been amended accordingly. Thus, withdrawal of the objection to the abstract is respectfully requested.

The specification stands objected to for failing to include a summary section. This objection is respectfully traversed. The cited rule states what a specification should include, and falls short of making a summary section mandatory. Intel Corporation has taken the position that they prefer to omit summaries in their applications. Since compliance with Rules 73 and 77 is entirely voluntary, it is respectfully suggested that the application is totally complete without a summary section, and therefore the requirement for a summary section is respectfully traversed.

The specification stands objected to for various informalities. The entire specification has been reviewed to identify any typographical errors. The specification has been amended to correct all such errors. Thus, withdrawal of the objection to the specification is respectfully requested.

Drawings:

The drawings stand objected to for various informalities. The drawings have been amended to correct these informalities, and formal drawings have now been submitted. Thus, withdrawal of the objection to the drawings is respectfully requested.

Claims:

Claims 10, 11, 13, 15-17 and 23 stand objected to for various informalities. Claims 10, 11, 13, 15-17 and 23 have been amended accordingly. Thus, withdrawal of the objection to the claims is respectfully requested.

Claims 1-4, 7, 10, 12-20, 23-26, 29, 32-34, 38-42 and 46 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Stark et al., "On Pipelining Dynamic Instruction Scheduling Logic" (Stark). Claims 5-6, 8-9, 11, 21-22, 27-28, 30-31 35-37, and 43-45 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Stark in view of Hennessy and Patterson, "Computer Architecture - A Quantitative Approach, 2nd Edition" 1996 (Hennessy). These contentions are respectfully traversed.

Independent claims 1, 23, 32 and 39 have been amended to clarify the claimed subject matter. The claimed speculative wakeup can be triggered by an instruction before selection of that instruction for execution is confirmed. As recited in claim 1: "A processor comprising: a wakeup loop to hold scheduler instructions including unexecuted instructions, and to indicate ready instructions of the unexecuted instructions that may be ready to be executed; at least one of the unexecuted instructions to wakeup and notify at least another of the unexecuted instructions to speculatively wakeup before selection

of the at least one of the unexecuted instructions is confirmed; and a select loop to select at least one of the ready instructions for execution." (Emphasis added.)

In contrast, the cited portions of Stark describe conventional scheduling in which dependent instructions are not woken up until their parent instruction(s) are confirmed as selected for execution. As described in Stark: "As shown in Figure 5, when both READY bits are set, the instruction requests execution. If the instruction receives a grant, its destination tag is broadcast on the tag bus. [...] Note that the wakeup and selection of the instruction straddles a clock edge. If the instruction is selected, the grant from the select logic gates the instruction's destination tag onto the tag bus, which is then fed to the tag comparators of the wakeup logic. Thus, the tasks of selection, tag broadcast, and wakeup must all occur within one cycle in order for dependent instructions to wakeup in consecutive cycles." (See Stark at page 61, sections 3.3 and 3.4.)

This cannot be considered speculative wakeup and is very different than the claimed subject matter. As described in the present specification, "With select-free scheduling logic, an instruction speculates that it will be selected for execution. The instruction asserts the AVAILABLE lines for its wakeup array entries before selection of the instruction is confirmed. [...]

Because there is usually no more than one instruction per wakeup array requesting execution, it is possible to speculate that any waking instruction will be selected for execution. Select-free scheduling logic exploits this fact by removing the select logic 102 from the critical scheduling loop and scheduling instructions speculatively. The select logic 102 is instead used to confirm that the schedule is correct. By breaking this loop, the processor cycle time is no longer set by the time required for wakeup and select, but is instead set just by the time required for wakeup." (See the present specification at pages 11-12, paragraphs 29-30; emphasis added.)

Stark describes breaking the conventional scheduling logic into a 2-cycle pipeline, with a latch added in the path of the select logic, tag broadcast, and wakeup logic. (See Stark at page 61, section 3.5.) In doing this, Stark describes a processor in which an instruction wakes up if either its parent instructions or its grandparent instructions have been selected for execution. (See Stark at page 62, section 4.) However, even this second processor described in Stark requires an instruction to be confirmed as selected before it can trigger wakeup for a child or grandchild instruction.

Independent claims 23, 32 and 39 have been amended in a similar manner as claim 1. With respect to independent claim 15, the art of record fails to teach or suggest "a select-free

scheduler", as claimed. The schedulers described in Stark require that instruction selection occur in order to trigger instruction wakeup. These schedulers cannot be considered select-free.

Thus, independent claim 1, 15, 23, 32 and 39 are in condition for allowance. Dependent claims 2-14, 16-22, 24-31 and 40-46 are patentable based on the above arguments and their own merits. For example, with respect to claim 16, the art of record fails to teach or suggest a processor having two schedulers, where a first of the two schedulers handles instructions with execution latencies less than a total scheduling latency, and a second of the two schedulers handles instructions with execution latencies greater than or equal to the total scheduling latency.

It is respectfully suggested for all of these reasons, that the current rejection is totally overcome; that none of the cited art teaches or suggests the features which are now claimed, and therefore that all of these claims should be in condition for allowance. A formal notice of allowance is thus respectfully requested.

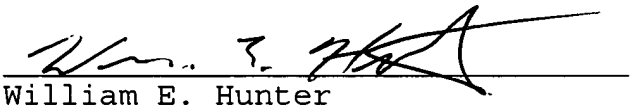
It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific issue or comment does not signify agreement with or concession of that issue or comment. Because the arguments made above may not be

exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

No fees are believed due with this response. Please apply any necessary charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 12/23/04



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